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Multilevel H-Bridge Dynamic Voltage Restorer with Harmonic Elimination

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Abstract: *This paper presents a new multilevel h- bridge-type dynamic voltage restorer (MHBDVR) with fault harmonic elimination. This topology can operate in two operational modes: 1) compensation mode for voltage fluctuations and unbalances, and 2) short- circuit current limiting mode. The harmonic eliminating function of the MHBDVR is performed by injecting third order harmonics during the short- circuit fault. By injection method we can reduce common mode voltage and reduced harmonic peak to peak level voltage to fundamental voltage The mathematical model of the MHBDVR system is also established in this paper. The control scheme design and optimal parameter selection are outlined based on the detailed theoretical analysis of the converter. Simulation results based on the MATLAB software and experimental results on a laboratory setup help to validate the proposed topology and the theoretical analysis.*

Index Terms: *Dynamic voltage restorer (DVR), multilevel inverters, fault current limiter, voltage restoration*

I. Introduction

There are two major challenges that modern power grids must deal with: voltage fluctuations and short-circuit faults[1]-[2]. There are renewable energy based generators (e.g. wind, solar) in the grid that can have varying output generation capabilities. Furthermore, the exponentially increasing power demand and popularity of distributed generation have resulted in increasing fault current levels.

A dynamic voltage restorer (DVR) could generate a compensation voltage, which is inserted into the grid through a series transformer [3-5], and could help to minimize any voltage fluctuations. However, a large short-circuit current will be induced into the voltage-source inverter (VSI) through the series transformer during faults. To overcome this problem, one alternative is a bypass scheme. It is a "fail safe" system in which the DVR can be taken off line [6]. Another approach is to improve the efficiency of the DVR [7]. The control schemes shown in [7] allow the series compensator to achieve load-side voltage restoration for upstream faults, and current limiting for downstream faults.

The disadvantage of this approach is that a large-capacity storage system is necessary at the DC side. Moreover, the proposed topology consists of a varistor and a couple of anti-parallel thyristors, which are connected in parallel to the secondary winding of the series transformer [8]. The principal protection element is a varistor, and the low- saturation magnetic characteristics of the series transformer are difficult to achieve. Nevertheless, the topology only protects the series VSI from the over- current and does not limit large currents from flowing in the system [9].

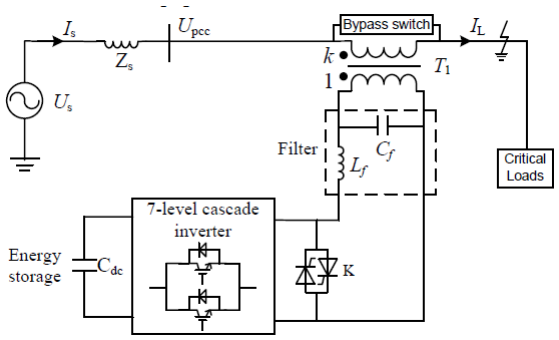
On the other hand, there are different topologies for fault current limiters (FCLs), such as superconducting FCLs, solid-sate FCLs, and resonance-type FCLs [10]-[11]. However, the additional equipment inevitably leads to an increase in the overall investment and capital cost. Hence, a better choice is improving the traditional functionality of the DVR to also limit the short-circuit current. The series compensator could complete the multiple functions by adding a new branch [12]-[13]. Furthermore, the proposed DVR can adjust the power factor through a thyristor- switched inductor branch [12]. Moreover, a common technique is where the bypass is connected in parallel to the primary of the series transformer [13]. The equipment consists of a bypass electronic switch, made up of anti- parallel thyristors, and a mechanical bypass switch which allows the static series compensator (SSC) to be bypassed [14]. Although the SSC is protected during faults, the fault-current is not limited to the desired value.

A fault current limiting dynamic voltage restorer (FCL- DVR) was proposed in [15]. However, the transient state of the FCL-DVR was not described in detail. The thermal stability and maximal withstand voltage of the current- limiting module were also ignored. The optimal parameter selection of the series transformer ratio has not been taken in [15]. On the other hand, a high power multilevel inverter produces lower harmonic currents, and requires lower rating power switches [16]-[18]. These aforementioned points are of great significance for the design and application of the multifunctional system.In this paper, a new

multilevel h-bridge-type dynamic voltage restorer (MHBDVR) is introduced to reduce theratio of the transformer. The MHBDVR provides similar cascade inverter performance benefits, such as the lower power rating and cost of the power devices used. Moreover, it limits the short-circuit current quickly during faults, and offers more effective protection to the system. The contents of the paper are organized as follows: the topology of the MHBDVR and its current-limiting function are described in Section II. In Section III, an effective control scheme and optimal parameter selection for the MHBDVR are proposed. In Section IV, the transient response state is studied in detail. In Section V, simulations and experimental results of the proposed MHBDVR are provided. Finally, the main conclusions are presented in Section VI.

II. Mhbdvr Topology

The MHBDVR system based on multilevel inverters is shown in Fig. 1. It consists of a series-connected transformer T_1, an energy storage capacitor C_{dc}, a seven- level cascade inverter, and a filter. The transformer T_1 not only reduces the voltage requirement of the inverters, but also provides isolation between the inverter and the utility grid. There are also anti-parallel thyristors K, which are the main difference between the MHBDVR and traditional DVRs [19]. In most practical inverters, there is also a bypass switch connected in parallel with the injection transformer [18]. Importantly, the energy storage capacitor (C_{DC}) provides the required power to compensate for any voltage sag or fluctuation in the utility grid. Although low-order harmonics are eliminated by the cascaded H-bridge, a large number of high-order harmonics are still present close to the equivalent switching frequency [18], [20]. As a result, an LC filter comprising of L_f and C_f is used as the filter for the cascaded multilevel DVR, as well as an impedance to limit the fault current. Thus the LC filter can achieve two different functions, and this will help to promote the full utilization of the equipment.



A. Function of the MHBDVR

Under the normal operating condition, the anti-parallel thyristors are not fired. Thus, the proposed MHBDVR is effectively seen as only comprising of the H-bridge cascade DVR. This multilevel converter not only realizes the higher power and voltage ratings using smaller rating switches, but also reduces the overall harmonic content. In addition, it contributes to a smaller dv/dt in the output and thus reduces unwanted electromagnetic interference [21]. On the other hand, when a short-circuit fault occurs along the distribution line, the load current increases sharply. The thyristors are then activated to insert the filter into the main current path through the series transformer. The filter, the series transformer and the anti-parallel thyristors together form a variable impedance that operates as the current- limiting module. The fault current is limited to the desired value, and the components of the VSI and other equipment in the system can be protected. As the voltage across the series transformer is not the same in the different modes, the mathematical model of the MHBDVR is

$$U_{\text{DF-DVR}} = k\alpha U_{dc}\,\text{sgn}(x) + Z_{\text{lim}} I_{fault}(1-\text{sgn}(x)) \qquad (1) \qquad (2)$$

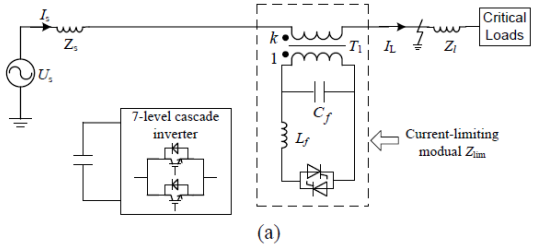
where U_{dc} is the dc-link voltage, k is the turns-ratio of the series transformer, and α is the modulation depth. Importantly, sgn(x) is the return function, and x is any valid value. For example, if the system is in the voltage regulation mode, x=1 and sgn(x)=1. Thus (1) can be rewritten as
Instead, if the system is in the current-limiting mode, x=0 and sgn(x)=0. Then (1) can be rewritten as

$$U_{\text{DF-DVR}} = Z_{\text{lim}} I_{fault}. \qquad (3)$$

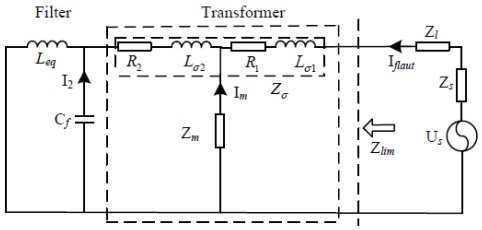
B. Current Limiting by the MHBDVR

The single-phase equivalent circuit of the MHBDVR in current-limiting mode is shown in Fig. 2. When a short- circuit fault occurs, the IGBTs of the faulted phase in the VSI are turned off and the cascade

inverter is shut down. Then, the thyristors are activated. Thus, the filter is inserted into the main current path through the series transformer T_1, as shown in Fig. 2(a).



(a)



(b)

The short-circuit current during the fault is then

$$I_{fault}(t) = \frac{U_s(t)}{Z_s + Z_l + Z_{\lim}} \approx \frac{U_s(t)}{Z_{\lim}} \qquad (4)$$

where Z_{lim} is the limiting impedance. As $Z_{lim} >> Z_S + Z_l$, the I_{fault} is mainly determined by the magnitude of Z_{lim}. Consequently, it can be limited to the desired value to protect the equipment in the system. Z_{lim} is determined by $L_{\sigma 1}$, $L_{\sigma 2}$, R_1, R_2, L_m, C_f, and k. $L_{\sigma 1}$ and R_1 are the leakage reactance and resistance of the primary side respectively $L_{\sigma 2}$ and R_2 are the leakage reactance and resistance of the secondary side respectively. Z_m is the excitation impedance of the transformer. Furthermore, the influences of Lσ1, R1, Lσ2, R2 can be ignored. It can then be concluded that the limiting impedance is

$$|Z_{\lim}| \approx k^2 \left(|j\omega L_{eq}| \,//\, |(1/j\omega C_f)| \,//\, |Z_m| \right). \qquad (5)$$

where L_{eq} is the equivalent impedance and therefore

$$L_{eq} = L_f \cdot \frac{\pi}{2\pi - 2\delta + \sin 2\delta} \qquad (6)$$

where δ is the trigger delay angle of the thyristors. Hence, the short-circuit current can be limited to the desired value by suitable selection of α, Lf and k

III. Control Scheme Design And Optimal Parameter Selection

The MHBDVR can operate in one of the two operation modes according to the state of the grid. In this section, the control scheme design and optimal parameter selection are explained.

A. Control Scheme

The primary drawback of the H-bridge inverter is the possibility of accidentally short-circuiting the input dc- link voltage by simultaneously switching on both transistors in a leg of the inverter. This is why, in such converters, a dead time is typically introduced to avoid this shoot-through and large over currents. New cascade inverters have also been proposed to solve this shoot- through problem, and they can greatly improve the overall system reliability [22-23]. In this paper, the cascaded H- bridge inverter is adopted as it is in wide use [16], [24].

When the MHBDVR is in the voltage compensation mode, it consists of a multilevel inverter with Three H- Bridge cells in each phase (synthesizing a 7-level output voltage), a small filter at the ac side, and three dc link capacitors. One of the main advantages of this topology, compared to other multilevel

topologies, is that the maximum number of levels is only limited by isolation constraints. Moreover, the modular structure of the converter leads to advantages in terms of manufacturing and overall system flexibility [24].Quite a lot of research has been conducted on the control methods of cascade inverter-based DVRs [5], [12]-[16]. The phase-shifted PWM is a widely used modulation strategy for cascaded multilevel inverters as it offers an even power distribution among the cells and is very easy to implement independent of the number of inverters. This modulation shifts the phase of each carrier by a suitable angle to reduce the overall harmonic content of the output voltage [25]. As it offers numerous benefits, the outlined inverter design and modulation strategy are used in this paper. Moreover, the voltage compensation control strategy for a MHBDVR system, as described in [4], is used.

When the MHBDVR is in fault current-limiting mode, it operates as discussed previously. This paper mainly focuses on the fault current detection method and the transient state of the fault current limiting operation mode. A fault current detection method is developed to sense the load current and its rate of change. The fault current is consequently limited to an acceptable level rapidly, even before reaching its first peak [26]-[27]. The schemes of the unbalanced disturbance are adopted [15], and are not discussed in this paper for brevity. The details of the transient state of the MHBDVR are described further in Section IV.

B. Optimal Parameter Selection

1) Cascaded inverter design: Using a PWM control strategy, the switches in the multilevel inverters should satisfy the following conditions

$$N_S \geq (U_{dvr} / n) / kU_r \qquad (7)$$

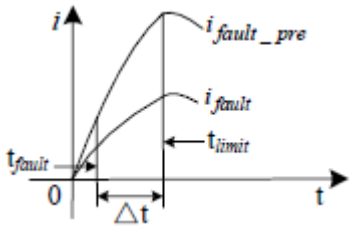
$$N_P \geq (kI_L) / I_r \qquad (8)$$

where N_S and N_P are the number of series switches in each inverter level and parallel branches in each leg of the
inverter respectively. U_{dvr} is the rated peak value of the series injected voltage of the MHBDVR. I_L is the rated value of the load current. U_r and I_r are the rated blocking voltage and the rated current of each switching component respectively. n is the total number of inverter levels in each phase. Then, the rated DC-link voltage of each
inverter level U_{dch} should meet
From (7)-(9), the overall minimum capacity of the switching devices can be obtained

$$U_{dvr} / n \leq U_{dch} \leq N_S U_r . \qquad (9)$$

$$S_{min\_total} = nN_{S\_min}N_{P\_min}U_r I_r \geq U_{dvr} I_L \qquad (10)$$

where N_{S_min} and N_{P_min} are the minimum values of N_S and N_P respectively. S_{min_total} is the total minimum capacity of the multilevel inverters. It can be concluded that the capacity
of the switching device, which is depended on U_r and I_r, can be altered by setting the values of the turns-ratio k, N_{S_min} and N_{P_min}.



When a short-circuit fault occurs (e.g. a three-phase to ground fault), the fault current will be 6-10 times that of the normal load current. Let us assume that the fault current is λ times greater than the load current in steady state. When a short-circuit fault occurs, the secondary current is kλ times greater than that of the load current. The ratio of the series transformer is 8:1 in [15], while the ratio is reduced to 3.5:1 in this paper. The change in the fault current at different transformer ratios is shown in Fig. 3. The fault occurs at t_{fault}, and MHBDVR enters into the current-liming mode at t_{limit} current during the preliminary period of the fault (where the limit module is not in series with the line) can be reduced. Overall, this will help to reduce the impact on the IGBTs and dc bus capacitor. After tlimit, the MHBDVR enters the limiting mode and the fault current is limited to the desired value.

2) Fault-current limiting module design: When the MHBDVR operates in the fault current limiting mode, the fault current will flow through the series transformer T1, LC output filter, and the bidirectional thyristors. The series transformer withstands the supply voltage during the faults, and hence the capacity of the series transformer is

$$S_T \geq U_S I_{fault} . \qquad (11)$$

In addition, the thermal stability of Lf, and the maximal withstand voltage of Cf should be considered during the faults. This relation is expressed as:

$$Q_{L_f} \geq \int_{t_{\text{fault}}}^{t_{\text{return}}} (k i_{fault})^2 dt \qquad (12)$$

Where QLf is the thermal stability of Lf during the fault. tfault and treturn are the time of the fault occurring and disappearing respectively. As the filter capacitor can be easily damaged by the overvoltage,

$$U_{C_f} \geq \max(u_{S\max} / k, u_{\text{dc}}) \qquad (13)$$

Where UCf is the maximal withstand voltage of the filter capacitor. udc and uSmax are the dc voltage and the maximum voltage across the series transformer respectively.

When the thyristors are deactivated, the voltages between the thyristors are the same as the output voltage of the cascade converter. The maximum value of the output voltages is approximately equal to the DC side voltage, while the current flowing through the thyristors is zero. When the thyristors are activated during the fault, the current flowing through the thyristor is k times of the fault current at the primary side. Thus, the thyristors can be given by where Qthy is the thermal stability of the thyristors, and Uthy is the maximal withstand voltage of the thyristors. Also, ucf is the voltage of the filtering capacitors and ucf = us/k.

3) Ride-through capability**:** Assuming that the magnitude of the voltage sag (with no phase-angle jump) is Usag in pu, the MHBDVR should inject an active power given by

$$Q_{\text{thy}} \geq \int_{t_{\text{fault}}}^{t_{\text{return}}} (k i_{fault})^2 dt \qquad (14)$$

$$U_{\text{thy}} \geq \max(u_{cf}, u_{\text{dc}}) \qquad (15)$$

$$P_{\text{DVR}} = -C_{\text{dc}} u_{\text{dc}} du_{\text{dc}} / dt = \sqrt{3} U_L I_L \cos\varphi_L (1 - U_{\text{sag}}) \qquad (16)$$

to restore the pre-sag rated voltage UL at the load terminals [14]. Here, the load current IL and the power factor φL are assumed to be constant. Furthermore, is the rated load power. If tsag is the voltage sag duration, the energy to be supplied by the MHBDVR is

$$W_{\text{DVR}} = \int_{t_0}^{t_0+t_{\text{sag}}} (-C_{\text{dc}} u_{\text{dc}} \frac{du_{\text{dc}}}{dt}) \text{dt} = \int_{t_0}^{t_0+t_{\text{sag}}} P_{\text{L}} (1 - U_{\text{sag}}) dt \qquad (17)$$

Then,

$$-C_{\text{dc}} [u_{\text{dc}}^2 (t_0 + t_{\text{sag}}) - u_{\text{dc}}^2 (t_0)] / 2 = P_L t_{\text{sag}} (1 - U_{\text{sag}}) . \qquad (18)$$

If the initial dc-link voltage is assumed to be its rated value, then udc(t0)=Udc0. Also, udc(t0+tsag)=kdUdc0 where kdUdc0 is the minimum allowable dc-link voltage at the end of the voltage sag (0<kd<1). Thus, in order to compensate the maximum voltage sag magnitude for a maximum expected sag duration Usag,max, the capacitance should be

$$C_{\text{dc}} \geq 2 P_L t_{sag,\max} (1 - U_{\text{sag,max}}) / U_{\text{dc0}}^2 (1 - \text{k}_{\text{d}}^2) . \qquad (19)$$

Increasing Udc0 allows the reduction of the size of the dc capacitor, but the choice of that voltage also depends on the maximum voltage rating of the H-bridge power electronic devices. Furthermore, the capacitor voltage rating also limits the maximum injection voltage. Two balancing schemes are adopted [28], and are not discussed in this paper for brevity.

4) LC design**:** Although the equivalent switching frequency of the cascade multilevel inverter is very high (e.g. 15 kHz), there are several higher harmonic components near the equivalent switching frequency. To attenuate these components and effectively lower the ripple voltages and currents, a LC based filter is proposed

$$R_L = 3U_{dc}^2 / P_{DVR} \quad (20)$$

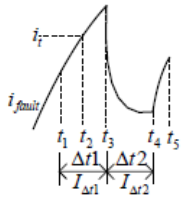
Hence, the resonance frequency is

$$f_c = 1/2\pi\sqrt{L_f C_f} = \sqrt{L_f / C_f}/2\pi L_f \quad (21)$$

$$\begin{cases} L_f = \rho / 2\pi f_c \\ C_f = L/\rho^2 = 1/2\pi f_c \rho \end{cases} \quad (22)$$

IV. Transient State Analysis

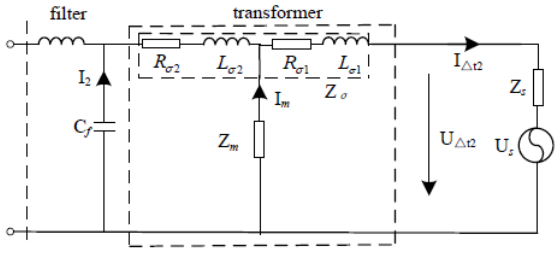
A. From Compensation Mode to Current-Limiting Mode



The forward switching scheme (from the compensation mode to the current-limiting mode) is to isolate the VSI from large currents during faults. The scheme achieves this by rapidly adding a limiting impedance in series with the transmission line to limit the short-circuit current to the desired value. As the scheme involves the state changes of the multilevel inverters and thyristors, the forward switching sequence is given in Fig. 4.

When a short-circuit fault occurs at t1, the line current increases rapidly. Once the current magnitude exceeds a preset threshold it (which depends on the relay protection) at t2, the IGBTs are turned off to completely deactivate the inverter. Considering the sensing time of the fault detector, the dead-time and non-ideal characteristics of the switches, the IGBTs are actually turned off at t3. Then, the control system gives a trigger signal to the thyristors at t4. Considering the non-ideal characteristics of the thyristors, the path K through the thyristors is in conduction at t5. Then, the forward switching is finally completed.(1) During $\Delta t1$, the fault current mainly depends on the system impedance Zs, and the leakage impedance Zσ of the series transformer [30]. Thus,From Fig.4, it is evident that the fault current $I\Delta t1$ increases sharply. The duration time $\Delta t1$ is very important to other devices and hence a fast fault current detection method is necessary. (2) During $\Delta t2$, the MHBDVR includes the supply power Us, the series transformer, and the filter capacitor Cf. The equivalent circuit is shown in Fig. 5. Thus,

$$I_{\Delta t2}(t) = U_{\Delta t2}(t) / |Z_m| + U_{\Delta t2}(t) / |1/j\omega C_f| \quad (24)$$



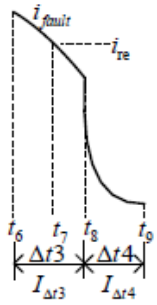
(3) During the switching process of the thyristors, the fault current will increase. After the thyristors are activated, the fault current Ifault is determined mainly by the limiting impedance Zlim, as given in (5). From (4) and (25), as Zlim
is much smaller than Zm and, Ifault is larger than $I\Delta t2$.

B. From Current-Limiting M o d e to Compensation Mode

The backward switching scheme (from the current- limiting mode to the compensation mode) is to turn off the thyristors after the fault. This scheme involves the state changes of the multilevel inverters and the thyristors, and the backward switching sequence is given in Fig. 6.

The short-circuit fault disappears at t6. If the magnitude of the load current is less than the return current i_{re} at t7, the control system removes the trigger signal to the thyristors. i_{revv}Is the reference value of the fault detection, and is larger Than the peak value of the load current. When the voltage across the thyristors is negative in polarity and the current is under the maintaining current, the thyristors are turned off at t8. Then, all of the IGBTs in the inverter are turned on at t9. Thus, the thyristors are still activated for the period Δt3 (from t_6 to t_8) and are turned off during Δt4 (from t_8 to t_9).

$$I_{\Delta t1}(t) = U_s(t) / (|Z_s + Z_\sigma|) . \qquad (23)$$

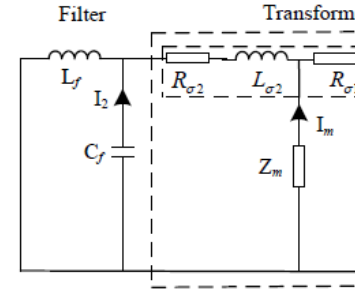


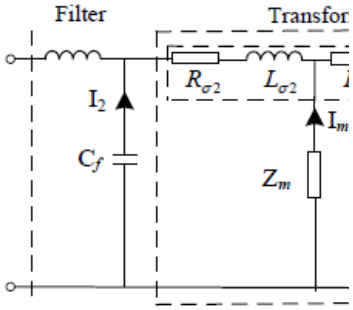
(1) During Δt3, the fault disappears. The equivalent circuit is shown in Fig. 7. It includes the power supply U_S, the

Limiting modules, and the load Z_{Load}. Ignoring Z_S and Z_l, the voltage across the current-limiting module is

As the leakage impedance Z_σ is ignored,

$$I_{\Delta t3}(t) = U_{\Delta t3}(t) / (|Z_m // (1/ j\omega C_f) // j\omega L_f|) . \qquad (26)$$





(2) During Δt4, the thyristors and the IGBTs also are turned off. The equivalent circuit of the system is shown

in Fig. 8. It includes the supply power U_S, the series transformer, and the load Z_{Load}. Thus, the load current is

$$I_{\Delta t4}(t) = U_{\Delta t4}(t) / (|Z_m // (1/ j\omega C_f)|) . \qquad (27)$$

After the backward switching sequence, the line current will recover to the normal value.

V. Simulation Results

To verify the feasibility of the MHBDVR, simulations are run using PSCAD/EMTDC software. The system simulation model is shown in Fig.1. The MHBDVR is connected in series between the supply network and the protected load. The corresponding parameter values used for the simulation are given in Appendix A. The supply voltage is assumed to be 10kV and the source is assumed to have a reactance of 100Ω. This corresponds to a fault level of 1MVA. In the simulations, while a seven-level cascade inverter is adopted, several high-order harmonics are still present near the equivalent switching frequency. As a result, an LC filter should be considered in the cascaded H-bridge. If a THD of 5% is considered as a threshold for the load voltage, the proposed method can meet the requirement. Moreover, the seven-level cascade inverter can successfully ride-through both balanced and unbalanced faults for voltage dips down to 80% at the converter terminals for 243 ms.

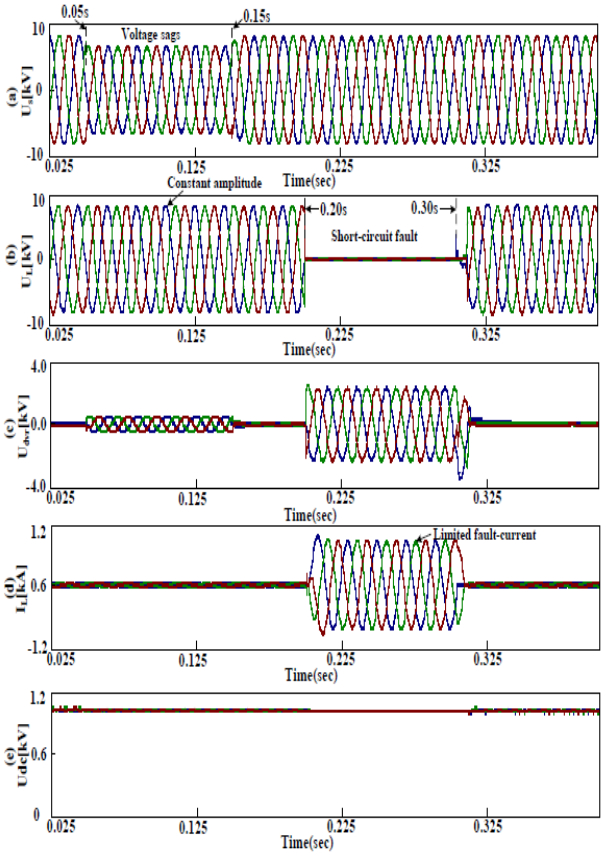


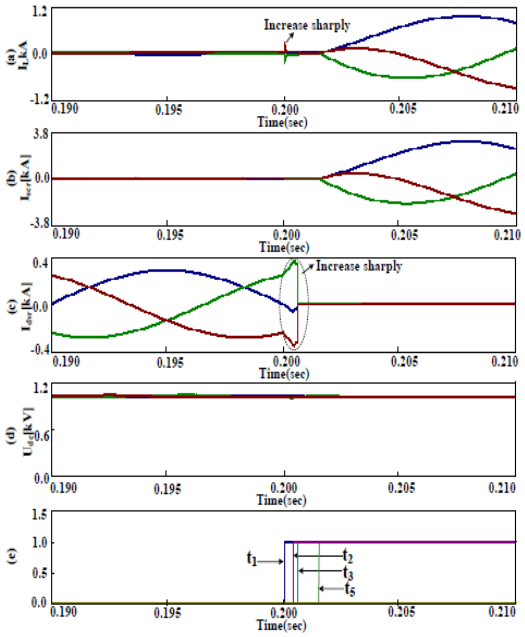
Fig.9. shows the performance of the MHBDVR under voltage sags and faults. As shown in Fig 9(a), a voltage sag occurs between 0.05s and 0.15s with a depth of 20%.

In Fig 9(b), it is observed that the load voltage U_L is regulated to a constant amplitude during this voltage sag.

The system is then subjected to a three-phase downstream fault by grounding the three-phase supply for 0.1s (i.e. five cycles). The load side voltage is nearly zero during the fault (from 0.2s to 0.3s), as almost all the voltage would drop across the current-limiting module as shown in Fig. 9(b)-(c). The load current will be quickly limited to the desired value due to the current-limiting function as shown in Fig. 9(d). Although the dc-link voltage drops slightly at 0.2s, it returns to its normal value immediately as shown in Fig. 9(e).

A. Forward Switching Simulations

When the transient fault occurs at t_1=0.2s, the load current increases sharply. The MHBDVR enters into the current- limiting mode before the amplitude of the fault current reaches its first peak. The simulation results of the forward Switching scheme are shown in Fig. 10. Considering the fault detection delay



time, the load current IL rises suddenly before t_2 as shown in Fig. 10(a). All the IGBTs are turned off at t_2. From Fig. 10(c),

Fig. 10(a). All the IGBTs are turned off at t_2. From Fig. 10(c), the output current I_{dvr} of the VSI increases from t_1 to t_2. The control system provides trigger signals to the thyristors at t_2. During $t_3<t<t_5$, the fault current is calculated using (24) and is very small. After the thyristors are activated at t_5, the fault current is determined by the current-limiting module. Therefore, when $t_1<t<t_5$, the output current of the VSI increases first before decreasing. Fig. 10(d) shows that the dc-link voltage increases slightly during the forward switching sequence.

B. Backward Switching Simulations

Assuming that the transient fault is cleared at t_6=0.3s, the MHBDVR enters into the DVR mode and can achieve the voltage regulating function during sags. The simulation results of the backward switching scheme are shown in Fig. 11.

Considering the time taken to detect that the fault has disappeared, locking signals are only given to the thyristors at t_7 in the simulations. Due to the half- controlled characteristic of the thyristors, they are only turned off completely at zero-crossing points. As discussed previously, the IGBTs are activated at t_8. Therefore, when $t_8<t<t_9$, the output currents of the VSI are calculated using (27). Fig. 11(d) shows that the dc-link voltage remains unchanged at 0.310s.

VI. Experiment And Analysis

The above simulations have demonstrated the validity of the proposed MHBDVR. To further verify the feasibility of the topology, experimental implementation and testing of the MHBDVR are presented in this section. Considering that the key feature of the MHBDVR is the transient state, which is between the DVR mode and the current limiting mode, the lab sample focuses on the testing of this function. The scaled-down single-phase H- bridge VSI is taken for this experimental study. The source is from a voltage regulator and its ratio is approximately 220V/110V. The IGBT used for this laboratory setup is the FF450R12ME4 driven with a switching frequency of 6.4kHz. The thyristors are MTC600A/12E. It is to be noted that the design value of the filter inductance L_f is 1.5mH and C_f is 20μF. L_0 is 1.5mH. The series-transformer ratio k is 1 with a 5 kVA capacity. The load resistance is 20ohm in normal operation. The phenomenon of the ground fault is simulated by paralleling a resistance of 5ohm with the load resistance, and hence the equivalent resistance is 4ohm during the fault.

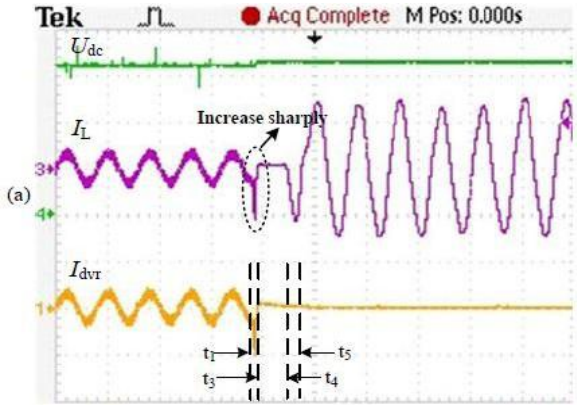
A. Forward Switching Experiment

The experiment to test the forward switching is shown in Fig. 12(a) where the fault occurs at t_1.

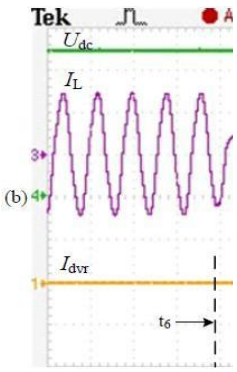
Consequently, the load current increases sharply from t_1 to t_3. When the fault is detected, the IGBTs are disabled. The fault current is very small from t_3 to t_4. The thyristors are activated at t_5. During $t_1<t<t_5$, the load current initially increases, then decreases before increasing once again. This phenomenon could be explained using (23) and (24). The dc-link voltage increases slightly during this forward switching experiment. Comparing Fig. 10(a), (c)-(d) and Fig.12 (a), the trend of the experimental waveforms closely resembles that of the simulation results.

B. Backward Switching Sequence Experiment

The experimental testing of the backward switching scheme is shown in Fig. 12(b). Here, the fault disappears at time t_6. Considering the half-controlled characteristic of the thyristors, they are only turned off completely at zero- crossing points. Thus the thyristors are disconnected after t_8. The load current I_{Load} can be decided by (26) during $t_6<t<t_8$, and it is small during $t_8<t<t_9$ according to (27).



The MHBDVR enters into the voltage regulation mode after t_9. The dc-link voltage rises slightly during the backward switching experiment. From Fig.11 (a),(c)-(d) and Fig. 12(b), the trend of the experimental waveforms are once again consistent with those of the simulation waveforms.



VII. Conclusions

Cascaded multilevel inverters have been applied in the industry as a cost-effective means of series sag compensation. However, a large current will be induced into the VSI through a series transformer during faults, and this is harmful to the VSI and the other equipment in the grid. In this paper, the MHBDVR was proposed to deal with voltage sags and short-circuit current faults. The MHBDVR has not only the advantages of the H-bridge cascade inverter, but also reduces the secondary side current in the preliminary period of the fault. A mathematical model of this system was also established in this paper. A careful analysis of the transient state verified the feasibility of the proposed MHBDVR. Based on the theoretical analysis, MATLAB simulations and the experimental results, we can conclude the following:

1) The H-bridge cascade inverter can be adopted to reduce the series transformation ratio and the secondary current during the preliminary period of the fault.
2) The transient state of the MHBDVR system was introduced in great detail.
3) The proposed control method can limit fault current with two cycle. The consistencies between the

simulation results and experimental results help to verify the proposed topology and theoretical analysis.

Appendix A

Source parameters: U_S=10kV, Z_S=1.21Ω, f_0=50Hz. Line: Z_{line}=0.340Ω. Load parameter: 1MW resistive Load MFSC parameters: seven-level cascade inverter. Switching frequency: 5kHz. DC link capacitor (per H-bridge module) C_{dc}=10000μF. LC filter inductor L_f=2mH. LC filter capacitor C_f=15μF. Series transformer ratio: 3.5:1. Leakage reactance: 0.1p.u. No load losses: 0.1 p.u. Magnetizing current: 0.4%.

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